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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,051	02/02/2000	Sywe N. Lee	6762-103XX	7019
167	7590	01/20/2004	EXAMINER	
FULBRIGHT AND JAWORSKI L L P			HENN, TIMOTHY J	
PATENT DOCKETING 29TH FLOOR				
865 SOUTH FIGUEROA STREET			ART UNIT	PAPER NUMBER
LOS ANGELES, CA 900172576			2612	
DATE MAILED: 01/20/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/497,051	LEE ET AL.	
	Examiner	Art Unit	
	Timothy J Henn	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 February 2000.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2 and 4-7 is/are rejected.
- 7) Claim(s) 3 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 - a) The translation of the foreign language provisional application has been received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. Figures 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: The specification refers to items 22 and 23 in Figure 2A starting on page 7, line 26, and item 24 in Figure 2B starting on page 10, line 9. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:
- i. On page 1, line 20: change "a CMOS active pixel sensors (APS) has" to "CMOS active pixel sensors (APS) have".
 - ii. On page 2, lines 13 and 14: move "and USP 5,900,623" to be before "both of which were assigned".
 - iii. On page 5, line 19: insert "the number" between "half" and "of".

- iv. On page 11, line 32 and page 12, line 5: the amplifier transistor is T5 in the figures, not T4.
- v. On page 12, line 10: the reset transistor is T1 in the figures, not T5.
Appropriate correction is required.

Claim Objections

4. Claims 2, 5 and 6 are objected to because of the following informalities: claims 2, 5 and 6 state that the invention comprises "two access transistors coupled in parallel to said source follower", however referring back to the specification and in particular, Figure 2B, it is seen that the two access transistors T3 and T4 are only in parallel with each other, and are not in parallel with the source follower transistor T2. For the purposes of art rejection, claims 2, 5 and 6 will be read as "two access transistors coupled in parallel to each other and connected to the output of said source follower transistor". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mimura (US 6,249,643) in view of Ochi (US 4,542,409).

[claim 1]

7. In regard to claim 1, note that Mimura discloses an image sensor for sensing light of an image, said image sensor comprising a plurality of first (Figure 1, Item "n LINE") and second (Figure 1, Item "n+1 LINE") elements arranged in rows and columns for generating respective analog signals in proportion to the intensity of the light impinging respectively on each of the light detecting elements (Column 2, Line 64 – Column 3, Line 3), characterized in that the first and second light detecting elements in each row of the sensor are alternately disposed (Figure 2(b), the examiner notes that each row of first and each row of second elements are alternately disposed in a vertical direction) and in that the first and second light detecting elements in two adjacent rows are disposed in a serrated manner (Figure 2(b), the examiner notes that in two adjacent rows, n and n+1, the first and second elements are offset to form a serrated pattern). Therefore, it can be seen that Mimura lacks first read lines to generate odd field signals and second read lines to generate even field signals, by selectively activating the first and second light detecting elements of the sensor.

8. It is further noted that Mimura generates an interlaced readout by performing a "zigzag" readout of the array (Figure 5(a)), and changing the position of a switch (Figure 4, Item 78) to alter the output position of the current cell being read. Ochi suggests a simpler method for interlaced readout in which first and second read lines are used to read out even and odd field signals respectively (Figure 5, Items V_A and V_B), ~~with~~ ^{which}

results in simplified interlaced readout (Column 6, Lines 10-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the readout line pattern of Ochi with the image sensor of Mimura to obtain an image sensor with is capable of simplified interlaced readout.

[claim 4]

9. In regard to claim 4, note that the first light detecting elements comprising two access transistors (Ochi, Figure 5, Items 73-1 and 73-2) coupled in parallel are activated by first (Ochi, Figure 5, Item 52) and second read (Ochi, Figure 5, Item 51) lines respectively, connected at the respective gates thereof, and wherein each of the second light detecting elements comprise two access transistors coupled in parallel and activated by the first read line (Ochi, Figure 5, Item 52) and another second read line (Ochi, Figure 5, Item 53), respectively, connected at the respective gates thereof.

[claim 7]

10. Claim 7 is a method claim corresponding to apparatus claim 1. Therefore, claim 7 is analyzed and rejected as previously discussed with respect to claim 1.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mimura (US 6,249,643) in view of Ochi (US 4,542,40) as applied to claim 1 above, and further in view of Ackland et al. (US 5,576,763).

[claim 2]

12. In regard to claim 2, the interlaced readout image sensor of Mimura in view of Ochi comprises photocells which include a photodiode and two access transistors

coupled in parallel (Ochi, Figure 5). Therefore, it can be seen that Mimura in view of Ochi lacks light detecting elements comprising a reset transistor and a source follower connected to the two parallel access transistors.

13. Ackland discloses an active pixel cell for use in an image sensor, which includes a reset transistor (Figure 3, Item 120; Column 4, Lines 19-22) to allow resetting of the cell and a source follower (Figure 3, Item 125; Column 4, Lines 31-34) to buffer the output of the cell. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the photo cell of Mimura in view of Ochi with the reset transistor and source follower of Ackland to include the benefits of resetting and buffering as taught by Ackland.

14. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ackland et al. (US 5,576,763) in view of Ochi (US 4,452,409).

[claim 5]

15. In regard to claim 5, note that Ackland et al. discloses a light detecting element for use in a CMOS active pixel image sensor (Figure 1) comprising a translating means comprising a reset transistor (Figure 1, Item 120) for resetting the initial state of a photodiode in the light detecting element (Column 4, Lines 19-22), a source follower (Figure 1, Item 125) for buffering an analog signal (Column 4, Lines 31-34) and a select or "access" transistor (Figure 1, Item 130; Column 4, Lines 36 and 37). Therefore, it

can be seen that Ackland et al. lacks two access transistors coupled in parallel to each other and connected to the output of the source follower transistor.

16. Ochi teaches a solid state imager, which uses FET access transistors coupled in parallel to each other (Figure 5, Items 73-1 and 73-2; Column 5, Lines 35-52) in order for the pixel cell to be read-out by two separate read lines. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the single access transistor Ackland et al. with the two parallel access transistors of Ochi to allow the pixel cells of Ackland et al. to be able to be read-out by two separate read lines.

[claim 6]

17. In regard to claim 6, note that the parallel access transistors of Ochi (Figure 5, Items 73-1 and 73-2) are coupled in parallel and are activated by a first read line (Figure 5, Item 51) connected to the gate of the first access transistor and a second read line (Figure 4, Item 52) connected to the gate of the second access transistor as claimed.

Allowable Subject Matter

18. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

[claim 3]

19. In regard to claim 3, the prior art does not teach or fairly suggest a readout of light detecting elements in which the elements in two adjacent rows activated by second

read lines substantially have average vertical location between the two adjacent rows and wherein the components of the first and second field signals are correlated with one another.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art further shows the current state of the art in image sensor interlaced readout.

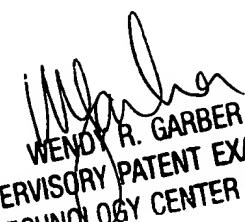
- | | | |
|----|---------------|--------------|
| a. | Nadler | US 4,471,387 |
| b. | Endo et al. | US 5,446,493 |
| c. | Sasaki et al. | US 5,581,357 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Henn whose telephone number is (703) 305-8327. The examiner can normally be reached on M-F 7:30 AM - 5:00 PM, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TJH
1/12/2004



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